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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Steve Nishimoto	§	Group Art Unit:	2189
		§		
Serial No.:	09/541,780	§		
		§	Examiner:	Christopher E. Lee
Filed:	April 3, 2000	§		
		§		
For:	Circuit and Technique to Stall the Communication of Data Over a Double Pumped Bus	§	Atty. Dkt. No.:	ITL.0349US (P8539)
		§		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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REPLY BRIEF

Dear Sir:

The following Reply is submitted to the Examiner's Answer.

I. CLAIMS ON APPEAL

Based on the Examiner's Answer, claims 1-14 and 20-23 have been allowed. Therefore, the remaining appealed claims include claims 15 and 17-19 grouped together; and claim 16 that is separately patentable for reasons set forth in the Appeal Brief.

II. REPLY TO EXAMINER'S ARGUMENT

In the Reply Brief, the Examiner contends that it would have been obvious for one skilled in the art to combine Tjandrasuwita, Applicant's Admitted Prior Art (AAPA) and Sproch to derive the invention that is set forth in claim 16. However, the Examiner fails to establish a *prima facie* case of obviousness for claim 16 for at least two reasons.

Date of Deposit:	June 9, 2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.	
Janice Munoz	

First, the Examiner fails to show with specific citations where the prior art contains the alleged suggestion or motivation to combine Sproch with either Tjandrasuwita or AAPA, and thus, for at least this reason, fails to establish a *prima facie* case of obviousness for claim 16. *Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143.

The Examiner fails to establish a *prima facie* case of obviousness for claim 16 for at least the additional, independent reason that even assuming, *arguendo*, that the combination of Tjandrasuwita, Sproch and AAPA is proper, the combination of these references fails to teach or suggest all limitations of claim 16. More specifically, the Examiner relies on Sproch to allegedly teach the disabling of alternate stages to prevent the communication of bits from a particular data flow. However, contrary to the Examiner's contentions, Sproch teaches pipeline stages that are clocked by a circuit 230. Instead of teaching disabling alternate stages of this pipeline architecture, Sproch teaches blocking communication of particular data flowing through the pipeline architecture by following the data through the architecture and disabling each stage through which the data propagates. *See, for example*, Sproch, 8:50-61. However, such a disclosure does not teach or suggest the missing claim limitations, i.e., the disabling of alternate stages to prevent the communication of bits from a particular data flow. Therefore, for at least the additional, independent reason that the combination of references fails to teach or suggest all claim limitations, a *prima facie* case of obviousness has not been established for claim 16.



The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0349US).

Date: 6/09/03

Respectfully submitted,

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APPENDIX OF CLAIMS

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The claims on appeal are:

1. An apparatus comprising:

a first circuit to receive indications of first data associated with a first data set and second data associated with a second data set; and

a second circuit coupled to the first circuit to cause the first circuit to:

in a first mode, communicate indications of the first data to an output terminal in synchronization with a first phase of a clock signal and communicate indications of the second data to the output terminal in synchronization with a second phase of the clock signal, and

in a second mode, communicate the indications of the first data to the output terminal in synchronization with the first phase and prevent communication of the second data during the second phase.
2. The apparatus of claim 1, wherein the first circuit comprises:

a first latch to store at least one bit at a time of the first data; and

a second latch to, at least in the first mode, store at least one bit at a time of the second data.
3. The apparatus of claim 2, wherein the first latch transfers said at least one bit of the first data in response to a predefined edge of the clock signal.
4. The apparatus of claim 2, wherein, in the first mode, the second latch transfers said at least one bit of the second data in response to a predefined edge of the clock signal.

5. The apparatus of claim 4, further comprising:
logic to selectively provide the clock signal to the second latch based on whether the apparatus is in the first or second mode.
6. The apparatus of claim 5, wherein the logic does not provide the clock signal to the second latch in the second mode.
7. The apparatus of claim 5, wherein the logic comprises:
an AND gate including a first input terminal to receive a mode select signal, a second input terminal to receive the clock signal and an output terminal coupled to a clock input terminal of the second latch.
8. The apparatus of claim 2, further comprising:
a multiplexer including an output terminal that is coupled to the output terminal of the apparatus, the multiplexer alternatively selecting the first and second latch in response to the first and second phases of the clock signal.
9. The apparatus of claim 1, wherein the apparatus comprises a double pumped bus circuit.

10. A computer system comprising:
- a system memory; and
 - a processor coupled to system memory, the processor including:
 - a wire;
 - a first circuit to receive indications of first data associated with a first data set and second data associated with a second data set; and
 - a second circuit coupled to the first circuit to cause the first circuit to:
 - in a first mode, communicate indications of the first data to the wire in synchronization with a first phase of a clock signal and communicate indications of the second data to the wire in synchronization with a second phase of the clock signal, and
 - in a second mode, communicate the indications of the first data to the wire in synchronization with the first phase and prevent communication of the second data during the second phase.
11. The computer system of claim 10, wherein the first circuit comprises:
- a first latch to store at least one bit at a time of the first data; and
 - a second latch to, at least in the first mode, store at least one bit at a time of the second data.
12. The computer system of claim 11, wherein the first latch transfers said at least one bit of the first data in response to a predefined edge of the clock signal.

13. The computer system of claim 11, wherein, in the first mode, the second latch transfers said at least one bit of the second data in response to a predefined edge of the clock signal.

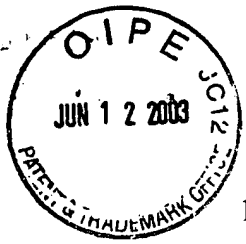
14. The computer system of claim 13, further comprising:
logic to selectively provide the clock signal to the second latch based on whether the apparatus is in the first or second mode.

15. A system comprising:
double pumped bus circuits serially coupled together to form a chain to communicate data from at least two different sets of data, at least one of the bus circuits being capable of being disabled to prevent bits from at least one of the sets of data from being communicated through said at least one of the bus circuits.

16. The system of claim 15, wherein alternate double pumped circuits are disabled to prevent the bits from at least one of the sets of data from being communicated through said at least one of the bus circuits.

17. The system of claim 15, wherein each double pumped circuit latches bits from one of the sets of data in response to first edges of a clock signal and furnishes indications of the bits in response to second edges of the clock signal, the first edges being different from the second edges.

18. The system of claim 17, wherein the first edges comprises positive edges of the clock signal.



19. The system of claim 17, wherein the first edges comprises negative edges of the clock signal.

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20. A method comprising:

receiving first indications of first data associated with a first data set;

receiving second indications of second data associated with a second data set;

in a first mode, communicating the first indications to a double pumped bus in synchronization with a first phase of a clock signal and communicating the second indications to the double pumped bus in synchronization with a second phase of the clock signal; and

in a second mode, communicating the first indications to the double pumped bus in synchronization with the first phase and preventing communication of the second indications to the double pumped bus during the second phase.

21. The method of claim 20, wherein the receiving the first indications comprises:

latching the first indications one bit at a time.

22. The method of claim 20, wherein the receiving the second indications comprises:

latching the second indications one bit at a time in response to the first mode.

23. The method of claim 20, wherein the communicating during the first mode comprises:

communicating bits of the first data in response to first predefined edges of the clock signal; and

communicating a bits of the second data in response to other predefined edges of the clock signal, said other predefined edges being different from the first predefined clock edges.